What is claimed is:

1. A program updating system having a communication function comprising:

a first processor which operates by referring to a program stored therein; and

a second processor which executes update of said program by using said communication function with an external unit, and executes an update control of said program when a fault of said first processor is detected.

2. The program updating system having the communication function according to claim 1,

wherein said second processor transmits a reset signal to said first processor for every predetermined cycles, and monitors a response pulse which is transmitted from said first processor in response to said reset signal, and transmits a compulsory reset signal to said first processor when said response pulse can not be detected within a predetermined period.

3. The program updating system having the communication function according to claim 2, further comprising:

an activation pulse generating circuit which generates an activation pulse to activate said second processor,

wherein said second processor starts transmitting of said reset signal in response to said activation pulse outputted from said activation pulse generating circuit.

4. The program updating system having the communication function according to claim 3, further comprising:

a buffer which transiently stores said program for executing said update control,

wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program in said buffer is completed.

5. The program updating system having the communication function according to claim 1, further comprising:

an activation pulse generating circuit which generates an activation pulse to activate said second processor,

wherein said second processor starts transmitting of said reset signal in response to said activation pulse outputted from said activation pulse

generating circuit.

6. The program updating system having the communication function according to claim 5, further comprising:

a buffer which transiently stores said program for executing said update control,

wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed.

7. The program updating system having the communication function according to claim 1, further comprising:

a buffer which transiently stores said program for executing said update control,

wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed.

8. The program updating system having the communication function according to claim 2, further comprising:

an activation monitoring circuit which generates an activation pulse to activate said second processor

and monitors transmission of an activation response pulse which is outputted from said second processor in response to said activation pulse,

wherein said activation monitoring circuit transmits a compulsory reset signal to said second processor when said activation response pulse can not be detected within the predetermined period.

9. The program updating system having the communication function according to claim 8, further comprising:

a buffer which transiently stores said program for executing said update control,

wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed.

10. The program updating system having the communication function according to claim 1, further comprising:

an activation monitoring circuit which generates an activation pulse to activate said second processor and monitors transmission of an activation response pulse outputted from said second processor in response to said activation pulse,

wherein said activation monitoring circuit

transmits a compulsory reset signal to said second processor when said activation response pulse can not be detected within the predetermined period.

11. The program updating system having the communication function according to claim 10, further comprising:

a buffer which transiently stores said program for executing said update control,

wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed.

12. A program updating method using a communication function, comprising:

providing a first processor which operates by referring to a program stored therein and a second processor,

transmitting a reset pulse from said second processor to said first processor;

transmitting a response pulse from said first processor to said second processor in response to said reset signal which is outputted from said second processor; and

transmitting a compulsory reset signal from said second processor to said first processor when said

response pulse can not be detected within a predetermined period to stop an operation of said first processor.

13. The program updating method using the communication function according to claim 12,

wherein said second processor transfers said program obtained by using said communication function to said first processor, during a stop of said first processor.

14. The program updating method using the communication function according to claim 13, further comprising:

providing an activation control circuit which controls activation and a stop of said second processor,

wherein said second processor transmits an activation response pulse to said activation control circuit for every predetermined cycles, and

said activation control circuit executes a stop control of said second processor, when said activation response pulse can not be detected within a predetermined period.

15. The program updating method using the communication function according to claim 12, further

comprising:

providing an activation control circuit which controls activation and a stop of said second processor,

wherein said second processor transmits an activation response pulse to said activation control circuit for every predetermined cycles, and

said activation control circuit executes a stop control of said second processor, when said activation response pulse can not be detected within a predetermined period.